Remarks

Applicant respectfully traverses the Office Action and submits amendments and responses as follows.

Objection to The Drawings

With respect to paragraph 1 in the Office Action, the Examiner reminds Applicant that figures 1-3b should be designated by a legend such as --Prior Art--. Accordingly, Applicant amends figures 1-3b by designating these figures with "Prior Art" legends, and reconsideration and withdrawal of these objections is therefore respectfully requested.

Claim Rejection - 35 U.S.C. § 102

With respect to paragraphs 2 and 3 in the Office Action, the Examiner rejected Claims 1-2, 4-5, 7, 9, 17, 19, 21, and 22 under 35 U.S.C. § 102(b) as being anticipated by Ker et al. (US 5,631,793). Of the rejected claims, claims 1, 17, and 21 are independent.

Applicant respectfully traverses this rejection. Ker et al. disclose a capacitor-couple electrostatic discharge (ESD) protection circuit for protecting an internal circuit and/or an output buffer of an IC form being damaged by an ESD current (Abstract). Particularly, Ker et al. focus on providing a bypass device to interconnect an input pad 21 to an internal circuit 23 (Fig.2), and such bypass device is only used in a single voltage source environment (Fig.3A-3D, Fig. 4A-4D, Fig. 5, Fig. 6, Fig. 7A-7D, Fig. 8, Fig. 9). It is to be noted that nothing about applications in mixed-voltage sources has been disclosed or taught by Ker et al.

In contrast, the present application focuses on providing an ESD prevention mechanism to protect areas supplied with different voltage levels in an IC with mixed-voltage sources. In such IC, power lines and power pins have to be independently separated to avoid noise coupling between "dirty" and "clean" buses. However, a situation of electrostatic discharge may happen between pins of any two circuits, i.e., the electrostatic discharge current may flow into the IC from one input or output pin and then flow out of the IC from the other pin. Therefore, the separate mixed-voltage power system would induce a different kind of ESD weakness as compared to the ESD problem in Ker et al. (background, 2nd paragraph of the present application). In such kind of ESD problem, using a resistance or back-to-back devices of the prior art still has problems.

Further, Ker et al. only designs a bypass circuit between one pair of VDD/VSS (Fig. 2, Ker et al.), but the RC controlled ESD circuit of the present application is connected to at least two pairs of Vcc1/Vss1, Vcc2/Vss2 (Fig.4, the present application). Therefore, the bypass circuit of Ker et al. is apparently different from the ESD circuit of the present application. In fact, the bypass circuit cannot function normally if it is directly installed on an IC with mixed voltage sources. Besides, Ker et al. does not teach anything to apply or adjust the bypass circuit to the IC with mixed voltage sources. Accordingly, Ker et al. does not disclose an identical circuit as the RC controlled ESD circuit of the present application, nor teach anything about the present application.

Besides, when applying 35 U.S.C. § 102, the following tenets of patent law must be adhered to:

"**A claim is anticipated only if <u>each and very element</u> as set forth in the claim is found, eith r expressly or inherently described, <u>in a single prior art reference</u>.**" *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "**The identical invention must be shown in <u>as complete detail as</u> is contained in the ... claim.**" *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). (MPEP §2131)

In addition, MPEP 2111.02 and cases, including In re Duva, 156 U.S.P.Q. (BNA) 90 (C.C.P.A, 1967) and Bell Communications Res., Inc. v. Vitalink Communications Corp., U.S.P.Q.2d (Fed Cir. May 1995), have held that statements in the preamble may not be disregarded in determining patentability. Therefore, all of the claim should be considered, including the preamble.

In the preambles of independent claims 1, 17, and 21 of the present application, "mixed voltage circuit assembly" are particularly pointed out. Further, in the bodies of these claims, "mixed voltage circuit assembly" is also combined tightly with elements of the subject matter. Therefore, in view of claims 1, 17, and 21 of the present application as a whole, "mixed voltage circuit assembly" should be considered in determining patentability of the present application. Because Ker et al. do not disclose anything about the "mixed voltage circuit assembly", Ker et al. does not anticipate claims 1, 17, and 21 of the present application.

Accordingly, the Applicant respectfully submits that independent claims 1, 17, and 21 are allowable over the art of record and respectfully requests the 35 U.S.C. § 102 (b) rejection of claims 1, 17, 21 to be reconsidered and withdrawn. In addition, insofar as claims 2, 4-5, 7, 9, 19,

and 22 respectively depend from independent claims 1, 17, 21 and add further limitations thereto, these claims should not be rejected under the 35 U.S.C. § 102 (b) as well.

Reconsideration and withdrawal of this rejection is respectfully requested.

Claim Rejection- 35 U.S.C. § 103

With respect to paragraphs 4 and 5 in the Office Action, the Examiner rejected claims 3, 8, 18, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Ker et al. The Applicant respectfully traverses this rejection as well as the cited patent and submits the following response.

Firstly, Ker et al. does not teach any device for preventing ESD between areas supplied with at least two different voltage sources. The bypass circuit of Ker et al. is designed only for a single voltage source IC, and the bypass circuit of Ker et al. does not function if the bypass circuit of Ker et al. is installed in an IC with mixed-voltage sources. The difference between Ker et al. and the present application is apparent. Besides, Ker et al. does not teach anything about the present application, and therefore, Ker et al. does not teach persons skilled in the art technical features of the present application.

In addition, when applying 35 U.S.C. § 103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be **considered as a whole**;

(B) The references must be considered as a whole and must **suggest the desirability** and thus the obviousness of making the combination;

(C) The references must be **viewed without the benefit of impermissible hindsight vision afforded by the claimed invention** and

(D) **Reasonable expectation of success** is the standard with which obviousness is determined.

Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986). (MPEP §2141)

With respect to independent claims 1, 17, and 21, "mixed voltage circuit assembly" is specifically pointed out in the preamble. Further, "mixed voltage circuit" is also tightly combined with elements in the bodies of claims 1, 17, and 21. Since Ker et al. do not teach nor suggest the desirability of "mixed voltage circuit assembly" at all, Ker et al. does not render obvious claims 1, 17, and 21 of the present application when considered as a whole. In addition, insofar as claims 3, 8, 18, and 22 respectively depend from independent claims 1, 17, and 21 and add further limitations thereto, these claims should not be rejected under the 35 U.S.C. § 103 (a) as well.

Reconsideration and withdrawal of this rejection is respectfully requested.

Other cited references of record have been studied, and are found no more relevant to the present invention than the applied art.

All claims in the present application are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

Conclusions

For all of the above reasons, the Applicant submits that the specification and claims are now in proper form, and that the claims define

patatentably over the prior art. Therefore the Applicant respectfully requests the Examiner to pass the case to issue.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,

LOWE HAUPTMAN GILMAN & BERNER, LLP

Benjamin J. Hauptman
Registration No. 29,310

1700 Diagonal Road, Suite 310
Alexandria, Virginia 22314
Telephone: (703) 684-1111
Facsimile: (703) 518-5499
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